

Claims

1. A semiconductor optical waveguide device comprising a semiconductor layer having an upper surface, and a lower surface which is defined by a lower confinement layer, the semiconductor layer having formed therein:
 - (a) a waveguide;
 - (b) at least one recess adjacent to the waveguide and extending from the upper surface of the semiconductor layer;
 - (c) at least one doped region, at least part of which is situated between a said recess and the lower confinement layer; and
 - (d) at least one trench adjacent to a said doped region and recess and situated on an opposite side thereof to the waveguide, wherein the (or each) trench extends from the upper surface of the semiconductor layer.
2. A device according to Claim 1, wherein the (or each) trench is deeper than its adjacent recess.
3. A device according to Claim 1 or Claim 2, in which the (or each) recess is spaced apart from its adjacent trench.
4. A device according to Claim 1 or Claim 2, in which the (or each) recess is not spaced apart from its adjacent trench, so that the recess and trench comprise a single larger feature.
5. A device according to any preceding claim, in which the (or each) doped region extends substantially to the lower confinement layer.

6. A semiconductor optical waveguide device comprising a semiconductor layer having an upper surface, and a lower surface which is defined by a lower confinement layer, the semiconductor layer having formed therein:
 - (a) a waveguide;
 - (b) at least one doped region extending substantially to the lower confinement layer; and
 - (c) at least one trench adjacent to, and spaced apart from, a said doped region and situated on an opposite side thereof to the waveguide, wherein the (or each) trench extends from the upper surface of the semiconductor layer.
7. A device according to any preceding claim, in which the (or each) trench extends substantially to the lower confinement layer.
8. A device according to any preceding claim, in which the waveguide is a rib waveguide, comprising a rib portion.
9. A device according to any preceding claim, in which the semiconductor comprises silicon.
10. A device according to any preceding claim, in which the lower confinement layer is a confinement layer for electrical charge carriers.
11. A device according to any preceding claim, in which the lower confinement layer is a confinement layer for an optical mode propagated by the waveguide.

12. A device according to any preceding claim, in which the lower confinement layer is an electrically insulating layer.
13. A device according to any preceding claim, in which the lower confinement layer comprises silica.
14. A device according to any preceding claim, in which there is a substrate layer below the lower confinement layer.
15. A device according to Claim 14, in which the substrate layer comprises silicon.
16. A device according to any preceding claim, in which there are two said doped regions, the doped regions being situated on opposite sides of the waveguide.
17. A device according to Claim 1 or any claim dependent thereon, in which there are two said recesses, the recesses being situated on opposite sides of the waveguide.
18. A device according to any preceding claim, further comprising an additional doped region.
19. A device according to Claim 18 when dependent upon Claim 8, in which the additional doped region is situated in the rib portion of the rib waveguide.

20. A device according to any preceding claim, in which there are two said trenches, the trenches being situated on opposite sides of the waveguide.
21. A device according to Claim 16 or any claim dependent thereon, in which the doped regions comprise n-doped and p-doped regions.
22. A device according to any preceding claim, which comprises a p-i-n diode.
23. A device according to Claim 22, which comprises a lateral p-i-n diode.
24. A device according to any preceding claim, which comprises an optical modulator.
25. An apparatus comprising a plurality of devices according to any preceding claim.
26. A device substantially as hereinbefore described and/or as illustrated in the accompanying drawings.